



Ali Azarpeyvand

Associate Professor

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Education

University of Tehran, Tehran, IR IRAN.

PhD in Computer Engineering (Computer Architecture) February 2014
Dissertation title: Reliability Analysis and Dependable Execution Techniques for Processors
in Nano-Scale Technologies
(*Nominated for the School of Engineering Best Doctoral Dissertation Award*)
Supervisors: Prof. Sied Mehdi Fakhraie and Prof. Saeed Safari

University of Tehran, Tehran, IR IRAN.

MSc degree in Computer Engineering (Computer Architecture) February 2000
Thesis title: Design and FPGA Implementation of the Baseband Part of Pager Receiver
Based on ERMES Standard
Supervisor: Prof. Sied Mehdi Fakhraie

Sharif University of Technology, Tehran, IR IRAN.

BSc degree in Computer Engineering (Computer Hardware) September 1997
Thesis title: Modeling of DLX RISC processor in dataflow level of abstraction
Supervisor: Prof. Shahin Hessabi

Research Interest

Compressed, Reliable and Secure Hardware Accelerators for DNN, Computer Architecture
Reliability Aware and Soft Error Resilient Systems, Dependability Analysis
Security Verification, Approximate Computing, Digital Systems Design

Professional Experiences

Senior Researcher (Post Doctoral)

(Sep. 2023 – Sep. 2025)

Tallinn University of Technology (TalTech), Tallinn, Estonia.

I'm working as a member of the Center for Dependable Computing Systems in the Department of Computer Systems at TalTech on the security verification and the design of compressed, reliable, and secure hardware accelerators for DNNs. As part of this work, I have utilized industry-standard EDA tools, including Cadence and QuestaSim, for digital design, verification, simulation, and hardware validation.

Projects:

Cross-level hardware security verification with semi-formal methods: Attacks are a top risk for organizations. This project develops a scalable, cost-effective security verification framework spanning from ISA to hardware, using assertion-based methods adapted from functional verification to improve security efficiently ([PSG837](#)).

Cross-Layer Reliability and Self-Health Awareness for Intelligent Autonomous Systems (CRASHLESS): CRASHLESS develops advanced reliability and self-health technologies for intelligent autonomous systems and IoT devices in Estonia and the EU. It addresses the complexity of AI-driven systems by enabling continuous self-monitoring and self-healing, providing tools for design and in-field operation ([PRG1467](#)).

Completed Projects:

AI-based quality control for the production of plastic bags: develop AI-driven process control for plastic bag production, which will enhance production efficiency and reduce energy consumption ([VEU22026IA5](#)).

President

(Feb. 2022 – Feb. 2023)

Zanjan Science and Technology Park, Zanjan, IR IRAN.

ZSTP encourages and supports innovation and R&D based start-ups and companies to be established and provide them with high-quality office area and support services. I managed a team of 25 employees and more than 100 start-ups.

Tenured Associate Professor

(Sep. 2021 – Present)

Tenured Assistant Professor

(Feb. 2014 – Sep. 2021)

Elec. and Comp. Engineering Department, University of Zanjan, Zanjan, IR IRAN.

Founder and Director

Advanced Computer Architecture and Embedded Systems Laboratory: Currently, the lab includes 8 PhD and 10 MSc students from computer and electrical engineering, all actively working on various projects. Additionally, more than 15 alumni, including 3 PhD graduates, have completed their studies.

Current Projects:

Reliability and Security Aware DNN Compression: Large amounts of layers and parameters made compression a necessary need. On the other hand, security and reliability of new silicons is challenging. Currently, several the innovative quantization and pruning methods are being implemented. Moreover, we are developing methods and platforms for security and reliability-aware DNN compression.

RISC-V Extension for DNNs: In recent years, the RISC-V processor has attracted significant attention. On the other hand, hardware accelerators for efficiently implementing deep neural networks have also become highly popular topics. Given the extensible nature of the RISC-V architecture, we are currently working on enhancing this processor by adding custom instructions, aiming to enable the use of deep neural networks on edge devices with limited resources.

Hardware Security Verification: Attacks on hardware especially on processors and hardware Trojans are increasing. In this project, we are working early detection of different hardware-based attacks such as Meltdown and Specter. Moreover, we are working on hybrid AI and ML-based algorithms for hardware Trojan detection and localization with high functional coverage and in a time-saved manner.

Completed Project:

Approximate Building Blocks: Approximate computing and inexact circuits are proposed as innovative and new solutions to reduce manufacturing costs, increase efficiency, and improve power consumption of digital circuits in applications such as image processing that inherently have the ability to tolerate errors in calculations. In this project, we are working to propose different imprecise computational building blocks such as adders and multipliers for use in image processing, DNNs, and similar applications.

Fault-Tolerant SOC: In this industrial project, we designed, implemented, and thoroughly tested a SPARC-based SOC along with a complete set of peripheral components developed from scratch, including UART, DMA, Timer, VIC, SDRAM Controller, and FPU. Additionally, we designed and fabricated a compact 10-layer mainboard to support the SOC, ensuring seamless integration and reliable performance. To facilitate software development and testing, we adopted a GCC-based compiler and debugger toolchain, enabling efficient code compilation and debugging for comprehensive validation of the system.

Director of the University IT Center:

(Sept. 2011 – Feb. 2022)

Research Deputy, University of Zanjan, Zanjan, IR IRAN.

I managed a team of 15 IT specialists responsible for supporting all aspects of the university's information technology infrastructure. Our responsibilities included maintaining and overseeing internet services, email systems, administrative automation, educational platforms such as Moodle, research management systems, and other related IT services. Under my leadership, the team ensured seamless operation, timely troubleshooting, and continuous improvement of these critical systems to support the university's academic and administrative functions efficiently.

Founder and Head of CERT team: (July 2016 – Sep. 2023)

Computer Emergency Response Team, University of Zanjan, Zanjan, IR IRAN.
As the Head of the university’s CERT, I led a team comprising 3 faculty members and over 10 graduate students from computer science and electronics disciplines. Together, we provided extensive cybersecurity services across the province, assisting various companies in threat mitigation, attack prevention, penetration testing, and incident response. Our team played a critical role in strengthening regional cybersecurity resilience and supporting organizations in safeguarding their digital asset.

Founder, Chief Executive Officer, and Project Manager (Feb. 2008 – Feb. 2022)

Tavana Information Processing System (TIPS) Company, Zanjan, IR IRAN.

www.tavanasys.com (company website in Persian)

With our technical team of over 135 computer engineers, we successfully developed more than 10 financial and security products and completed numerous custom projects tailored to our clients’ specific needs. Our company’s innovative solutions and strong market presence attracted the attention of a leading international financial group, which subsequently acquired the company and relocated its operations abroad. This transition marked a significant milestone, reflecting the value and impact of our technology and expertise in the global market.

Selected Projects:

Couple of financial projects including Online Trading System, Settlement and Clearing System, Investment Found System, BPMS, ..

Enterprise Social Network for Companies: A specialized platform designed for corporate environments that integrates all standard features of social media—such as user profiles, messaging, and content sharing—with essential business tools. These include project management and control, task scheduling, shared calendars, online meetings, and collaborative workspaces, enabling seamless communication and productivity within organizations.

Track of Secure hardware (Secure USB, Secure Flash, Secure Patch panel, Secure gateway)

Graduate Research Assistant (Feb. 2007 – Feb. 2014)

Silicon Intelligence and VLSI Signal Processing Laboratory,
Electrical and Computer Engineering Department, University of Tehran, Tehran, IRAN.
Supervisor: Prof. Sied Mehdi Fakhraie

Research problem: Soft Error Analysis and Resiliency for Processors

Contributions:

In my PhD, I proposed the Instruction Vulnerability Factor (IVF), a new metric for assessing the susceptibility of processor instructions to transient faults. This enabled a fast and efficient estimation of the Architectural Vulnerability Factor (AVF), useful for evaluating processor reliability during program execution. To support this, I developed the Configurable Reliability Analysis Framework (CRAF) for automated IVF analysis. I later extended IVF to extensible processors by introducing the Custom Instruction Vulnerability Factor (CIVF), allowing designers to select custom instructions based on fault vulnerability alongside performance and power metrics. A dedicated framework (CIVA) was also built to integrate CIVF into the design process.

Instructor (Sept. 2000 – Feb. 2007)
Elec. and Comp. Engineering Department, University of Zanjan, Zanjan, IR IRAN.

Head of Computer Engineering Department
Faculty of Engineering (Sept. 2001 – Aug. 2003) and (Sept. 2004 – Aug. 2005)

Contributions:
Managed a department with 10 faculty members, 300 undergraduate students and
Developed and taught new courses such as Hardware Description Languages and
VLSI.

Senior Digital Design Engineer (Jun. 1998 – May 2003)
Emad Semicon Co., Ministry of Industry, Tehran, IR IRAN.

Contributions: Managed a team of 10 engineers (Digital Systems).

Main Projects:
Design and FPGA implementation of several CPU cores (MIPS, ARM, SPARC)
Design and FPGA implementation of the baseband part of a pager receiver
Design and FPGA implementation of WPAN security suite
Design a 2/4 FSK Demodulator for paging applications with Automatic Frequency Control
Design Protocol Decoders for ERMES and FLEX
Design Controllers for I²C Bus, HDLC and CAN
FPGA implementation of a Direct Digital Frequency Synthesizer (DDFS)

Senior Digital Design Engineer (Sept. 2001 – Sept. 2002)
Advantage Design and Technology Co., Iran design office, Tehran, IR IRAN.

Main Projects:
Design a full digital calibrator for A/D converter
Develop a C program for converting Verilog netlist to Spice netlist
Synthesize a large design with cadence synthesis tool

Honors and Awards

Recipient of a Research Excellence Recognition at the University of Zanjan for the most-cited publication among faculty members	2026
Selected as distinguished lecturer of computer engineering department	2018,2019,2020,2025
Awarded the University of Zanjan the most valuable research project	2021
Selected as University of Zanjan Faculty member with the most research contracts	2021
Nominated for the University of Tehran Best Doctoral Dissertation Award	2013
Awarded Iran Nanotechnology Initiative Council grant for the PhD thesis	2010
Awarded Ministry of Science, Research & Technology grant for the PhD thesis	2009
Ranked 16 in the Iranian Nationwide Entrance Exam for Graduate Studies in the general field of computer engineering	1997
Ranked among the top 5% in the whole program of computer engineering B.Sc.	1997
Ranked 348 in the Iranian Nationwide Undergraduate College Entrance Exam	1993

Professional Activities

Reviewer:

IEEE Transactions on Reliability (TR)
IEEE Transactions on Computers (TC)
IEEE Transaction on VLSI (TVLSI)
IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
IEEE Transactions on Emerging Topics in Computing (TETC)
IEEE Transactions on Emerging Topics in Computational Intelligence (TETCI)
IEEE Transactions on Parallel and Distributed Systems (TPDS)
IEEE Transactions on Pattern Analysis and Machine Intelligence (TPAMI)
IEEE Transaction on Circuits and Systems I (TCAS-I)
IEEE Transaction on Circuits and Systems for Artificial Intelligence (TCASAI)
IEEE Transaction on Device and Materials Reliability (TDMR)
IEEE Transactions on Industrial Informatics (TII)
IEEE Transactions on Sustainable Computing (TSUSC-CS)
IEEE Sensors Journal
IEEE Access
ACM ACM Computing Surveys (CSUR)
ACM Transactions on Intelligent Systems and Technology (TIST)
ACM Transactions on Design Automation of Electronic Systems (TODAES)
Elsevier Engineering Applications of Artificial Intelligence
Elsevier Microelectronics Reliability
Elsevier Microelectronics
Elsevier Microprocessors and Microsystems
Springer Neural Computing and Applications
Springer Softcomputing
Springer Supercomputing
Wiley Concurrency and Computation: Practice and Experience
IET Circuits, Devices & Systems
IET Electronics Letters
IEICE Transactions on Information and Systems
Design, Automation & Test in Europe Conference & Exhibition (DATE)
IEEE European Test Symposium (ETS)

Executive Committee Member:

13th Iranian Conference on Electrical Engineering (ICEE 2013)

Member of Technical Program Committee:

8th Iranian Conference on Machine Vision and Image Processing (MVIP 2013)

Course Developments/Upgrades

New Courses (I started teaching these courses at the University of Zanjan):

Advanced Topics in DNNs, Graduate, Spring 2025
High-Performance Multiprocessor Systems, Graduate, Spring 2015
Embedded System Processing Elements, Graduate, Spring 2013

Software Fault Tolerance - Advance Topics, Graduate, Spring 2011
High-performance Computer Architecture, Graduate, Spring 2009
Hardware Description Languages (HDLs), Graduate, Fall 2001
Very Large Scale Integrated circuits, Senior Undergraduate, Spring 2001

Course Upgrade:

Digital Logic Design, Undergraduate, University of Zanjan Spring 2001

Description:

I enhanced this course by incorporating new content focused on digital design using Hardware Description Languages (HDLs) and Computer-Aided Design (CAD) tools. The updated curriculum included practical training with tools such as MaxPlus II and Verilog, providing students with hands-on experience in modern digital system design and simulation.

Software Tool Development

HAWX: A Hardware-Aware FrameWork for Fast and Scalable ApproXimation of DNNs
University of Zanjan, Fall 2025 (role: supervisor)

Goals: HAWX is a framework that rapidly finds the optimal balance between AI performance and hardware efficiency by intelligently deciding where to use faster, less precise components within a neural network.

SynAssert: Automated Synthesis of CSCA Leakage Patterns into Cost-Effective Security Assertions, Tallinn University of Technology, Fall 2024

Goals: Converting well-known Cache Side-Channel Attack Leakage Pattern to System Verilog Security Assertions.

CRAF: Configurable Reliability Analysis Framework, University of Tehran, Fall 2009

Goals: Estimating the vulnerability of processors to soft error

CIVA: Custom Instruction Vulnerability Analysis framework, University of Tehran, Fall 2011

Goals: A framework for analyzing the vulnerability of custom instructions to soft errors.

APPRICOT: Automatic Code Annotation for Approximate Computing, University of Zanjan, Spring 2017 (role: supervisor)

Goals: A framework for analyzing the source codes and automatically annotating code segments which are appropriate for approximation.

Teaching Experience

Associate Professor/Assistant Professor/Instructor at University of Zanjan:

Advanced Topics in DNNs, Spring 2025, 2026
Embedded Systems Processing Elements, Spring 2019, 2016, 2015, 2014, 2013
High-performance Computer Architecture, Fall 2025, 2024, ..., 2012
Advanced Digital Electronics, Fall 2019
High-performance Multiprocessor Systems, Fall 2015
Software Fault Tolerance - Advanced Topics, Fall 2010
Hardware Description Languages, Fall 2001, 2002, 2003, 2009, 2010
Digital Logic Design, For more than 30 semesters

Introduction to Computer Architecture, For more than 30 semesters
 Very Large Scale Integrated circuits (VLSI), Spring 2001
 Undergraduate project (thesis), more than 40 theses
 Digital logic design laboratory (Founder), Fall 2001 to Fall 2007.
 Computer Architecture laboratory (Founder), Fall 2002 to Fall 2007.
 FPGA laboratory (Founder), Fall 2004 to Fall 2007.

Technical Presentations

- SynAssert: Automated Synthesis of CSCA Leakage Patterns into Cost-Effective Security Assertions
 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2025)
 Kalamata, Greece. July 2025
- PATROL: An Evolutionary Approach to Automatic Test Pattern Generation for Hardware Trojan
 Detection Leveraging PSO-GA Hybrid Techniques
 33rd IEEE Asian Test Symposium (ATS 2024)
 Ahmedabad, Gujarat, India. May 2024
- AdAM: Adaptive Fault-Tolerant Approximate Multiplier for Edge DNN Accelerators
 29th IEEE European Test Symposium (ETS 2024)
 The Hague, Netherlands. December 2024
- Reliability Analysis and Dependable Execution Techniques for Processors in Nano-Scale Technologies
 Design, Automation, and Test in Europe (DATE 2017, PhD Forum)
 Presented by my colleague, Lausanne, Switzerland. March 2017
- Vulnerability Analysis for Custom Instructions
 15th Euromicro Conference on Digital System Design (DSD 2012),
 Izmir, Turkey. Sept. 2012
- Hardware implementation of the bit interleaver for the IEEE 802.22 standard
 20th Iranians Conference on Electrical Engineering (ICEE 2012),
 Tehran, Iran. May 2012
- CIVA: Custom Instruction Vulnerability Analysis framework
 IEEE 15th International Symposium on Design and Diagnostics
 of Electronic Circuits and Systems (DDECS 2012),
 Tallinn, Estonia. April 2012
- Reliability Considerations In Dynamic Voltage And Frequency Scaling Schemes
 IEEE 5th IEEE International Conference on Design & Technology
 of Integrated Systems in Nanoscale Era (DTIS 2010),
 Hammamet, Tunisia. March 2010
- Energy/throughput Trade-off In A Fully Asynchronous NoC For GALS-based MPSoC Architectures
 IEEE 5th IEEE International Conference on Design & Technology
 of Integrated Systems in Nanoscale Era (DTIS 2010),
 Hammamet, Tunisia. March 2010

References

Seid Mehdi Fakhraie, Professor (PhD thesis supervisor)

School of Electrical and Computer Engineering
University College of Engineering, University of Tehran
North Kargar Ave., Tehran, 14395-515, IR Iran

Unfortunately he passed away on December 2014

Jaan Raik, Professor (Postdoc supervisor)

Head of Centre for Dependable Computing Systems
Department of Computer Systems
Tallinn University of Technology
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Zain Navabi, Adjunct Teaching Professor (PhD advisor)

Electrical and Computer Engineering Department
Worcester Polytechnic University
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Saeed Safari, Associate Professor (PhD thesis co-supervisor)

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Ebrahim Rahimpour, Professor (Former colleague at the University of Zanjan)

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Alireza Khanteymoori, Associate Researcher (Former colleague at the University of Zanjan)

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Universitätsklinikum Freiburg
Neurozentrum, Freiburg, Germany
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Email: Alireza.khanteymoori@uniklinik-freiburg.de

Publications

Journal articles and conference papers under revision:

- Bahram Parchegani, Samira Nazari, **Ali Azarpeyvand**, et al., "CoG-Guided Weight Correction for Fault-Tolerant Deep Neural Networks," submitted to IEEE Transactions on Reliability.
- Babak Rokh, **Ali Azarpeyvand**, et al., "SPRUNN: Structural Proximity for Pruning in Deep Neural Networks," submitted to IEEE Transactions on Emerging Topics in Computing (Major revision has been submitted).
- Babak Rokh, **Ali Azarpeyvand**, et al. "HEAR-Net: Hardware-Efficient Weight Binarization with Adaptive Regularization for Deep Convolutional Neural Networks," submitted to Springer Softcomputing (Major revision has been submitted).
- Smaneh Rahimi, **Ali Azarpeyvand**, and Tara Ghasempouri "MRUSD: Maximally Redundant UnSigned Digit Number System," submitted to IEEE Transactions on Computer Aided Design (TCAD).
- Sara Makenali, Babak Rokh, and **Ali Azarpeyvand**, "Integrating Pruning with Quantization for Efficient Deep Neural Networks Compression," submitted to Image and Vision Computing.

Journal papers:

- Samira Nazari, **Ali Azarpeyvand**, and Mohsen Afsharchi, "GRADE: A Scalable Framework for Reliability Assessment of Deep Neural Networks in Safety-Critical Systems," in IEEE Transactions on Reliability, vol. 75, pp. 2379-2393, 2026, doi: 10.1109/TR.2026.3704288.
- **Ali Azarpeyvand**, et al., "ClearCache: Configurable Lightweight Early-stage AccuRate Cache Timing Side-Channel Attacks Detection Using Cache Global History Table", J Supercomput 82, 256 (2026), <https://doi.org/10.1007/s11227-025-08174-x>.
- Mahdi Taheri, Natalia Cherezova, Samira Nazari, **Ali Azarpeyvand**, et al., "AdAM: Adaptive Approximate Multiplier for Fault Tolerance in DNN Accelerators" IEEE Transactions on Device and Materials Reliability, vol. 25, no. 1, pp. 66-75, March 2025, doi: 10.1109/TDMR.2024.3523386
- S. Sharifian, V. Rashtchi and **A. Azarpeyvand**, "Parallel Chaos-based image encryption algorithm: High-Level Synthesis and FPGA implementation", Journal of Supercomputing, Vol. 80, No. 8, pp. 10985–11013, May 2024, doi: 10.1007/s11227-023-05784-1.
- Shima Pouyan, Mostafa Charmi, **Ali Azarpeyvand**, and Hossein Hassanpoor, "Propounding first artificial intelligence approach for predicting robbery behavior potential in an indoor security camera", IEEE Access, Vol 11, pp 60479-60489, 2023.
- Rokh, B., **Azarpeyvand, A.**, and Khanteymoori, A., "A Comprehensive Survey on Model Quantization for Deep Neural Networks in Image Classification", ACM Transactions on Intelligent Systems and Technology, Vol. 14, Issue 6, pp. 1-50, 2023.
- Samaneh Rezaei, Reza Omid, and **Ali Azarpeyvand**, "Logarithm-approximate floating-point multiplier", Microelectronics Journal, Vol. 127, Issue C, 105521, 2022.

- Omid Abbaszadeh, **Ali Azarpeyvand**, Ali Reza Khanteymoori, and Abbas Bahari, "Data-driven and Knowledge-based Algorithms for Gene Network Reconstruction on High-dimensional Data", *IEEE/ACM Transactions on Computational Biology and Bioinformatics (IEEE/ACM)*, Vol 19, Issue 3, pp. 1545-1557, 2022.
- Mohsen NourAzar, Vahid Rashtchi, **Ali Azarpeyvand**, and Farshad Merrikh-Bayat "Code Acceleration Using Memristor-Based Approximate Matrix Multiplier: Application to Convolutional Neural Networks", *IEEE Transaction on VLSI (IEEE)*, Vol. 26, Issue 9, pp. 2684-2695, 2018.
- Mohsen NourAzar, Vahid Rashtchi, Farshad Merrikh-Bayat and **Ali Azarpeyvand**, "Towards Memristor-based Approximate Accelerator: Application to Complex-Valued FIR Filter Bank", *Analog Integrated Circuits and Signal Processing Journal (Springer)*, Vol. 96, Issue 3, pp. 577-588, 2018.
- Omid Abbaszadeh, Ali Reza Khanteymoori, and **Ali Azarpeyvand** "Parallel Algorithms for Inferring Gene Regulatory Networks: A review", *Current Genomics (Bentham Science)*, Vol. 19, Issue 7, pp. 603-614, 2018.
- Mostafa E. Salehi, **Ali Azarpeyvand**, and Armin Hajaboutalebi, "Vulnerability Analysis of Adder Architectures Considering Design and Synthesis Constraints", *Journal of Electronic Testing (Springer)*, Vol. 34, Issue 1, pp. 7-14, 2018.
- Mohsen NourAzar, Vahid Rashtchi, **Ali Azarpeyvand**, and Farshad Merrikh-Bayat, "Memristor-based Approximate Matrix Multiplier", *Analog Integrated Circuits and Signal Processing Journal (Springer)*, Vol. 93, Issue 2, pp. 363-373, 2017.
- **Ali Azarpeyvand**, Mostafa E. Salehi, Seid Mehdi Fakhraie, and Saeed Safari, "Fast and Accurate Architectural Vulnerability Analysis for Embedded Processors Using Instruction Vulnerability Factor", *Journal of Microprocessors and Microsystems (ELSEVIER)*, Vol. 42, pp. 113-126, 2016.
- Fatemeh Pouyan, **Ali Azarpeyvand**, Saeed Safari, and Sied Mehdi Fakhraie, "Reliability aware throughput management of chip multi-processor architecture via thread migration", *The Journal of Supercomputing (Springer)*, Vol. 72, Issue 4, pp. 1363-1380, 2016.
- Fatemeh Pouyan, **Ali Azarpeyvand**, Saeed Safari, and Sied Mehdi Fakhraie, "Reliability-aware Simultaneous Multithreaded Architecture Using Online Architectural Vulnerability Factor Estimation", *IET Computers & Digital Techniques*, Vol. 9, Issue 2, pp. 124-133, 2015.
- **Ali Azarpeyvand**, Mostafa E. Salehi, and Seid Mehdi Fakhraie, "An Analytical Method For Reliability Aware Instruction Set Extension", *The Journal of Supercomputing (Springer)*, Vol. 67, Issue 1, pp. 103-130, 2014.
- F. Firouzi, **Ali Azarpeyvand**, M. E. Salehi, and S. M. Fakhraie, "Adaptive Fault-Tolerant DVFS with Dynamic Online AVF Prediction", *Journal of Microelectronics Reliability (ELSEVIER)*, Vol. 52, Issue 6, pp. 1197-1208, 2012.
- Amir M. Sodagar, G. R. Lahiji, and **Ali Azarpeyvand**, "Reduced-Memory Direct Digital Frequency Synthesizer Using Parabolic Initial Guess", *Journal of Analog Integrated Circuits and Systems (Kluwer Academic)*, Vol. 34, Issue 2, pp. 89-96, 2003.

Refereed conference papers:

- Samira Nazari, Mohammad Saeed Almasi, Mahdi Taheri, **Ali Azarpeyvand**, et al. "HAWX: A Hardware-Aware FrameWork for Fast and Scalable ApproXimation of DNNs", 2026 Design, Automation & Test in Europe Conference (DATE), Verona, Italy, 2026, pp. 1-7, doi: 10.23919/D-ATE69613.2026.11539476.
- Ali Soltan Mohammadi, Samira Nazari, **Ali Azarpeyvand**, et al. "RESQ: A Unified Framework for REliability- and Security Enhancement of Quantized Deep Neural Networks", 2026 IEEE 27th Latin American Test Symposium (LATS), Florianópolis, Brazil, 2026, pp. 1-4, doi: 10.1109/LATS70329.2026.11480282.
- Danial Monachan, Samira Nazari, Mahdi Taheri, **Ali Azarpeyvand**, et al., "Mix-and-Match Pruning: Globally Guided Layer-Wise Sparsification of DNNs", 12th International Conference on Computing and Artificial Intelligence (ICCAI 2026), to appear.
- Mostafa Hosseini, **Ali Azarpeyvand**, et al., "GUARD: An ABC-GA Hybrid Approach Utilizing MACHine LeaRning and Dimensionality Reduction for Hardware Trojan Detection", 2025 IEEE East-West Design & Test Symposium (EWDTS), Tbilisi, Georgia, 2025, pp. 1-8.
- Mohammad Reza Heidari Iman, Rolf Drechsler, Chandan Kumar Jha, **Ali Azarpeyvand**, et al. "Application of Functional Verification Techniques in Hardware Trust", Special Session, 38th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2025), Barcelona, Spain, 2025, pp. 1-8, doi: 10.1109/DFT66274.2025.11257462.
- Sharifian, S., Taheri, M., **Azarpeyvand, A.**, et al. "Reliability-Aware Hyperparameter Optimization for ANN-to-SNN Conversion", WiPiEC Journal - Works in Progress in Embedded Computing Journal, 11(1), 7, <https://doi.org/10.64552/wipiec.v11i1.85>.
- **Ali Azarpeyvand**, et al. "SynAssert: Automated **S**ynthesis of CSCA Leakage Patterns into Cost-Effective Security **A**ssertions," IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2025), Kalamata, Greece, 2025, pp. 1-6, doi: 10.1109/ISVLSI65124.2025.11130310.
- S. Nazari, M. Taheri, **A. Azarpeyvand**, et al. "Reliability-Aware Performance Optimization of DNN HW Accelerators Through Heterogeneous Quantization," 2025 IEEE 26th Latin American Test Symposium (LATS), San Andres Islas, Colombia, 2025, pp. 1-6.
- Mostafa Hosseini, **Ali Azarpeyvand**, et al., "SHIELD: PSO-Based Hardware Trojan DetectIon for Efficient and Low-Cost Defense", IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS 2025), Ischia, Italy, 2025, pp. 1-4.
- Samira Nazari, Mahdi Taheri, **Ali Azarpeyvand**, et al., "GENIE: GENetic Algorithm-Based REliability Assessment Methodology for Deep Neural Networks", 11th International Conference on Computing and Artificial Intelligence (ICCAI 2025), Kyoto, Japan, 2025, pp. 264-271.
- Samira Nazari, Mahdi Taheri, **Ali Azarpeyvand**, et al. "FORTUNE: A Negative Memory Overhead Hardware-Agnostic Fault TOLerance TechniqUe in DNNs", 2024 IEEE 33rd Asian Test Symposium (ATS), Ahmedabad, India, 2024, pp. 1-6.

- Mostafa Hosseini, **Ali Azarpeyvand**, and Tara Ghasempouri, "PATROL: An Evolutionary Approach to Automatic Test Pattern Generation for Hardware TROjan Detection Leveraging PSO-GA Hybrid Techniques", 2024 IEEE 33rd Asian Test Symposium (ATS), Ahmedabad, India, 2024, pp. 1-6.
- Bahram Parchegani, **Ali Azarpeyvand**, et al., "Zero-Memory-Overhead Clipping-Based Fault Tolerance for LSTM Deep Neural Networks", 2024 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Didcot, United Kingdom, 2024, pp. 1-4.
- Hossein Rostami, Mostafa Hosseini, **Ali Azarpeyvand**, et al., "Automatic High Functional Coverage Stimuli Generation for Assertion-based Verification", IEEE 30th International Symposium on On-Line Testing and Robust System Design (IOLTS 2024), Rennes, France, July 2024, pp. 1-7.
- Mahdi Taheri, Natalia Cherezova, Samira Nazari, Ahsan Rafiq, **Ali Azarpeyvand**, et al., "AdAM: Adaptive Fault-Tolerant Approximate Multiplier for Edge DNN Accelerators", 29th IEEE European Test Symposium 2024 (ETS 2024), The Hague, Netherlands, May 2024, pp. 1-4.
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